IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Recker et al.	Atty. Dkt.: SC11244ZC
Serial No.: 09/654,253	Group Art Unit: 2128
Filed: September 1, 2000	Examiner: DAY, Herng Der
Title: MISMATCH MODELING TOOL	

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Date: January 18, 2005

DECLARATION UNDER MPEP 608.01(p)

Sir:

In compliance with MPEP 608.01(p), this Declaration by Applicant's representative is a statement that the amendatory material added to the above referenced Patent Application consists of material that was originally incorporated in the Patent Application by reference to one or both of A Comprehensive MOSFET Mismatch Model by P. Drennan and C. Andrew, IEEE IEDM, 1999 and Integrated Circuit Device Mismatch Modeling and Characterization for Analog Circuit Design, - Ph. D. dissertation, Arizona State University, May 1999, by P. Drennan.

SC11244ZC Declaration by Bethards under 37 C.F.R. §1.132

I, Charles W. Bethards, the undersigned, do hereby depose and sayeth:

1. That I represent Freescale Semiconductor, Inc. and the Applicants before the Patent and Trademark Office in the above reference Patent Application, Serial Number 09/654,253.

2. That on information and belief a Response to a Final Office Action (dated November 17, 2004) concerning Patent Application, Serial Number 09/654,253, is being filed on January 18, 2005, that entry of Amendments to Patent Application, Serial Number 09/654,253, as identified in the Response are being requested, and that any material added by the Amendments was originally included in Patent Application, Serial Number 09/654,253 by reference to one or both of A Comprehensive MOSFET Mismatch Model by P. Drennan and C. Andrew, IEEE IEDM, 1999 and Integrated Circuit Device Mismatch Modeling and Characterization for Analog Circuit Design, - Ph. D. dissertation, Arizona State University, May 1999, by P. Drennan.

3. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the Subject Application or any patent which issues thereon.

Charles W. Bethards Dated: 1/18/05

Charles W. Bethards
Reg No 36,453